REMARKS

Applicant greatly appreciates the Examiner's finding of some allowable subject matter and appreciates the Examiner's effort to bring the case forward.

Applicant respectfully requests reconsideration and allowance of the subject application. Claims 21-57 are pending in this application.

Allowable Subject Matter

Applicant gratefully acknowledges that claims 25, 31, 33, 42, 43, 47, 49, and 57 are allowable if rewritten in independent form to include their base claims and any intervening claims. The claims are not rewritten in this response for the reasons provided below.

Objection to the Disclosure

An informality in the disclosure has been corrected by updating the "Related Applications" section. The citation of copending application 10/158,505, since it has issued, has been updated with its patent number, 6,731,148.

Claim Objections

Claim 58 was objected to informally for reciting "data transfer" of the first and second signals. Applicant, however, requests that claim 58 be canceled without prejudice, to advance the prosecution towards allowance.

Claim Rejections – 35 USC § 102

Claims 21-24, 26-30, 32, and 35-36

Claims 21-24, 26-30, 32, and 35-36 were rejected under 35 USC § 102(b) as being anticipated by Applicant's admitted prior art Figs. 1-3.

In an Examiner Interview held telephonically on March 2, 2005, Applicant reached agreement with the Examiner that this rejection should be removed. A summary of the Examiner Interview under MPEP § 713.04 follows:

SUMMARY OF SUBSTANCE OF EXAMINER INTERVIEW OF MARCH 2, 2005 UNDER MPEP § 713.04.

A telephonic interview was held on March 2, 2005 with participants Kenneth Wells, Examiner; and Mark Farrell, counsel for the Applicant.

Regarding the claim rejections under 35 USC § 102(b), Applicant pointed out that the delay locked loop in Figs. 1-3 (prior art) does not "generate" the first signal as is recited by Applicant's claims. Applicant's specification on page 2, lines 9-10 refers to the admitted prior art and states, "Lines 112a and 112b transmit a clock signal generated by a clock generator 120, coupled to line 112a." Claim 21, on the other hand, recites "...a delay locked loop to generate the first signal...", that is, in the claim, at least one of the clock signals is generated by the recited delay locked loop (not by the clock generator).

The Examiner agreed that this distinction should cause the 35 USC § 102(b) rejections as to Figs. 1-3 admitted prior art to be removed.

Claims 37, 40, 41, 44-46, 48, 51-52

Claims 37, 40, 41, 44-46, 48, 51-52 were rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,140,854 to Coddington et al. (the "Coddington reference").

Claim 37

Claim 37 defines a method of operation in a memory controller that includes:

"generating a first signal using a single delay-locked loop wherein the first signal is used to time data transmission;
changing a phase difference between the first signal and a reference signal by a first time period using a second delay element outside the feedback path of the delay-locked loop circuit; and
receiving a second signal to be delayed relative to the first signal by the first time period using a first delay element in a feedback path of the delay-locked loop, wherein the second signal is used to time data reception."

The Coddington reference, on the other hand, discloses a system that includes a shifting delay circuit that provides a variable delay for delaying a source clock and a delay-locked loop that includes a delay line providing a variable delay for delaying the source clock. The delay line has its delay varied by a counter, which is incremented in order to change the delay. The shifting delay circuit is based on half periods of a reference clock that has a known relationship to the source clock. The total delay for the source clock is a combination of that provided by the shifting delay circuit and the delay line.

The Coddington reference does not show the method of claim 37. That is, the Coddington reference does not specifically or inherently disclose Applicant's

first delay element in a feedback path of the delay-locked loop that receives a second signal, delays the second signal by a time period, wherein the second signal is used to time data reception; and a second delay element that is not in a feedback path of the delay-locked loop, that changes a phase difference between a first signal and a reference clock by the same time period as used on the second signal, wherein the first signal is used to time data transmission. Since the Coddington reference does not show the method of Applicant's claim 37, Applicant requests that the rejection under 35 U.S.C. § 102(e) be removed.

The Patent Office identifies elements of Applicant's method of claim 37 with the device shown in Coddington's Fig. 2. That is, the Office identifies Applicant's first signal with Coddington's clock at terminal 94; Applicant's single delay-locked loop with Coddington's circuit 70; Applicant's reference signal with Coddington's clock at terminal 52; Applicant's second delay element with either Coddington's "delay element" 90 or Coddington's "delay element" 91; Applicant's second signal with Coddington's feedback clock at terminal 97; and Applicant's first delay element with Coddington's element 92, holding that the functional limitations of claim 37 are all deemed to be inherent in the operation of Coddington's Fig. 2.

Applicant respectfully points out, however, that at least some of the Coddington components are identified by the Office in a manner different than identified by the Coddington reference itself. For example, the Office identifies Coddington elements 90, 91, and 92 as delay elements. Coddington, however, identifies elements 90, 91, and 92 as "output buffers" at col. 3, lines 60-61 and as "input buffers" at col. 4, line 16. Since, Coddington calls out delay lines explicitly, (such as "delay line 72"), identifying Applicant's delay elements with Coddington

buffers is objectionable. Specifically, identifying Applicant's first delay element with Coddington output buffer 92 and identifying Applicant's second delay element with either Coddington output buffer 90 or output buffer 91 is incorrect as the function of buffers and delay lines are different. For example, the Coddington buffers could not delay Applicant's first signal with respect to Applicant's reference clock by Applicant's time period, and simultaneously delay Applicant's second signal with respect to Applicant's first signal by Applicant's same time period. Accordingly, the device shown in Coddington's Fig. 2 could not perform Applicant's method defined in claim 37.

Claims 40, 41, 44-46, 48, 51-52

Claims 40, 41, 44-46, 48, 51-52 are dependent on base claim 37, and include the same limitations as claim 37. For at least the reasons explained above, namely that since the Coddington reference does not anticipate each and every element of Applicant's base claim 37, Applicant requests that the rejection under 35 U.S.C. § 102(e) also be removed from dependent claims 40, 41, 44-46, 48, 51-52.

Claim Rejections under 35 U.S.C. § 103(a)

Claim 34

Claim 34 was rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art Figs. 1-3 in view of either Erickson or Self.

Claim 34 is dependent on claim 21. The 35 U.S.C. 102(b) rejection of claim 21 based on Applicant's admitted prior art Figs. 1-3 has been removed by the Office in an Examiner Interview of March 2, 2005.

In order to present a prima facie case of obviousness, the combined references must teach or suggest all the elements of Applicant's claims. There is no teaching or suggestion in admitted prior art Figs. 1-3 to combine with either Erickson or Self to form the elements of Applicant's claim 21. Nothing in Applicant's admitted prior art Figs. 1-3, Erickson, or Self, taken singly or in combination, teaches or suggests, for example, a memory controller that includes a delay locked loop to generate a first signal on a first signal line, wherein the first signal is used to transmit data to a random access memory device, and a second signal received on a second signal line by the delay locked loop samples read data provided by the memory device, wherein the first and second signal lines are coupled to the memory device and to the memory controller.

Thus, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 34 be removed.

Claims 38, 39, 53-56, and 58

Claims 38, 39, 53-56, and 58 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Coddington et al. in view of Applicant's admitted prior art Figs. 1-3. Claims 38 and 39 are dependent on claim 37, while claim 53 is an independent claim and claims 54-56 are dependent on claim 53. Claim 58 has been canceled to advance the prosecution towards allowance. A response to the 35 U.S.C. § 102(e) rejection of claim 37 is given above. The admitted prior art Figs. 1-3 have been removed as a 35 U.S.C. § 102(e) reference in an Examiner Interview of March 2, 2005.

Additionally, a prima facie case of obviousness has not been presented by the Office, as the combined references must teach or suggest all the elements of

Applicant's claims. Even if the Coddington reference were valid for presenting a prima facie obviousness rejection, there is still no teaching or suggestion in the Coddington reference, for example, of the memory controller in claim 37 that includes a delay locked loop to generate a first signal on a first signal line, wherein the first signal is used to transmit data to a random access memory device, and a second signal received by the delay locked loop on a second signal line to sample read data provided by the memory device, wherein the first and second signal lines are coupled to the memory device and to the memory controller and delay with respect to a reference clock and to each other by the same time period. Likewise, there is no teaching or suggestion in the Coddington reference, with respect to claim 53, of a delay-locked loop that receives a second signal, wherein the delay-locked loop includes a first delay element coupled in a feedback path of the delay-locked loop, the first delay element changing a phase difference between the second signal and a reference clock signal by a first time period, and a second delay element outside the feedback path receiving the second signal and outputting a first signal that is delayed relative to the second signal by the first time period.

Claims 38 and 39 are dependent on base claim 37, while claims 54-56 are dependent on base claim 53, each discussed above. For at least the reasons given for base claims 37 and 53 above, the obviousness rejection should also be removed from claims 38, 39, 54-56.

Claim 50

Claim 50 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the Coddington reference in view of either Erickson or Self. Claim 50 is dependent on claim 37. The Coddington reference fails to support a rejection of claim 37 under 35

U.S.C. § 102(e) as argued above, as the Coddington reference does not anticipate each element of claim 37. Combining the Coddington reference with one or both of the Erickson reference and the Self reference does not cure the deficiency of the Coddington reference—none of these three references, alone or in combination, teaches or suggests all the elements of Applicant's claim 50.

Obviousness-type Double Patenting Rejection

Claims 21-58 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 6,371,148 and claim 7 of U.S. Patent No. 6,469,555. The Office Action states that "although the conflicting claims are not identical, they are not patentably distinct from each other because the instant claims are all anticipated by the inventions claimed in the previous two patents."

Claim 58 has been canceled to advance the prosecution towards allowance. Applicant respectfully traverses the double patenting rejection of claims 21-57. The two cited patents have claims that recite aspects of a single delay-locked loop that generates two different clock signals—one clock signal indicating when to read data from a bus and another clock signal indicating when to write data to the bus. The instant claims, on the other hand, recite yet another aspect of the subject matter: a memory controller that includes a delay locked loop to generate a first signal to transmit data to a random access memory device and to receive a second signal such that the second signal is used to sample read data provided by the memory device. Hence, the instant claims are patentably distinct over claims 1-20 of U.S. Patent No. 6,371,148 and over claim 7 of U.S. Patent No. 6,469,555.

Applicant therefore respectfully requests that the double patenting rejection be removed.

CONCLUSION

Applicant respectfully suggests that claims 21-57 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

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By: _____

Lee & Hayes PLLC
Mark C. Farrell
Reg. No. 45,988
(509) 324-9256